WHAT IS CLAIMED IS:

1. A multi-chip package comprising:

a rectangular first semiconductor chip having a first face on which a plurality of bonding pads are formed and a second face opposite to the first face;

a rectangular second semiconductor chip which is mounted on the first face of the first semiconductor chip and which has a first face on which a plurality of bonding pads are formed and a second face that faces the first face of the first semiconductor chip;

a plurality of leads electrically connected with the plurality of bonding pads of the first semiconductor chip or the plurality of bonding pads of the second semiconductor chip;

an auxiliary lead which supports the first semiconductor chip at a corner of the first face of the first semiconductor chip and which extends toward an outside of the first semiconductor chip; and

a sealant for sealing the auxiliary lead, part of the leads, the first semiconductor chip, and the second semiconductor chip.

2. The multi-chip package according to claim 1, wherein the auxiliary lead extends between extension lines of two sides of the first semiconductor chip that form a corner of the first semiconductor chip, the extension lines extending toward the outside of the first semiconductor

chip.

3. The multi-chip package according to claim 1, wherein a part of the auxiliary lead which externally extend out of the first semiconductor chip extends along a diagonal extension line of the first semiconductor chip.

4. The multi-chip package according to claim 2, wherein a part of the auxiliary lead which externally extend out of the first semiconductor chip extends along a diagonal extension line of the first semiconductor chip.

5. The multi-chip package according to claim 1, wherein the auxiliary lead is positioned in the vicinity of the corner of the first semiconductor chip and has a plurality of diverging portions that support the first face of the first semiconductor chip.

6. The multi-chip package according to claim 5, wherein the diverging portions of the auxiliary lead support the corner of the first semiconductor chip along sides of the first semiconductor chip.

7. The multi-chip package according to claim 1, wherein the auxiliary lead becomes gradually thick, as it extends toward an outside of the first semiconductor chip.

8. The multi-chip package according to claim 1, wherein the auxiliary lead is covered with an insulating protection film.

9. A multi-chip package comprising:

a rectangular first semiconductor chip having a first face on which a plurality of bonding pads are formed and a second face opposite to the first face;

a rectangular second semiconductor chip which is mounted on the first face of the first semiconductor chip and which has a first face on which a plurality of bonding pads are formed and a second face that faces the first face of the first semiconductor chip;

a plurality of leads electrically connected with the plurality of bonding pads of the first semiconductor chip or the plurality of bonding pads of the second semiconductor chip;

an auxiliary frame which supports a region surrounding corners of the first face of the first semiconductor chip and an outer periphery of the second semiconductor chip mounted on the first semiconductor chip and which extends toward an outside of the first semiconductor chip; and

a sealant for sealing the auxiliary frame, part of the leads, the first semiconductor chip, and the second semiconductor chip.

10. The multi-chip package according to claim 9, wherein the auxiliary frame is integrally formed.

11. The multi-chip package according to claim 9, wherein a part of the auxiliary frame which externally extends out of the first semiconductor chip extends along a diagonal extension line of the first semiconductor chip.

12. The multi-chip package according to claim 10, wherein a part of the auxiliary frame which externally extends out of the first semiconductor chip extends along a diagonal extension line of the first semiconductor chip.

13. The multi-chip package according to claim 9, wherein the plurality of bonding pads formed on the first semiconductor chip are arranged along four sides of the first semiconductor chip and positioned between an outer periphery of the first semiconductor chip and the auxiliary frame.

14. The multi-chip package according to claim 1, wherein the first semiconductor chip and the second semiconductor chip are arranged in such a manner that the first face of the first semiconductor chip and the first face of the second semiconductor chip may face each other.

15. The multi-chip package according to claim 9,

wherein the first semiconductor chip and the second semiconductor chip are arranged in such a manner that the first face of the first semiconductor chip and the first face of the second semiconductor chip may face each other.

16. The multi-chip package according to claim 15, wherein a plurality of bumps are formed on the plurality of bonding pads of the second semiconductor chip, a conductor which is electrically connected with each of the bumps is formed on the first semiconductor chip, and a wiring line for electrically interconnecting the conductor and part of the bonding pads of the first semiconductor chip arbitrarily is formed.

17. The multi-chip package according to claim 16, wherein the wiring line is formed in the first semiconductor chip.

18. The multi-chip package according to claim 9, wherein the auxiliary frame becomes gradually thick as it extends to an outside of the first semiconductor chip.